1. (Amended) A single electron transistor device comprising:

a source;

a drain;

a gate;

a buried gate layer of silicon nanoparticles; and

wherein said silicon nanoparticles have a diameter of approximately 1 nm.

5. (Amended) A method for operating a single electron device, which has a source, a drain, a gate, and 1nm diameter silicon nanoparticles implanted as a buried gate layer, comprising the steps of:

creating at least one hole in the silicon nanoparticles to enable the silicon nanoparticles to conduct a single electron at room temperature across the source and the drain; and

applying a voltage across the drain and the source.

6. (Amended) The method of operating the single electron device according to claim 4, wherein said step of creating a hole in said silicon nanoparticles is accomplished by irradiating said silicon nanoparticles.

7. (Amended) The method of operating the single electron device according to claim 5, wherein said step of creating a hole uses light having a spectral width between 300nm and 600nm.

8. (Amended) A transistor memory device comprising:

a source;

a drain; and

a gate, with 1nm diameter silicon nanoparticles contained in a control oxide